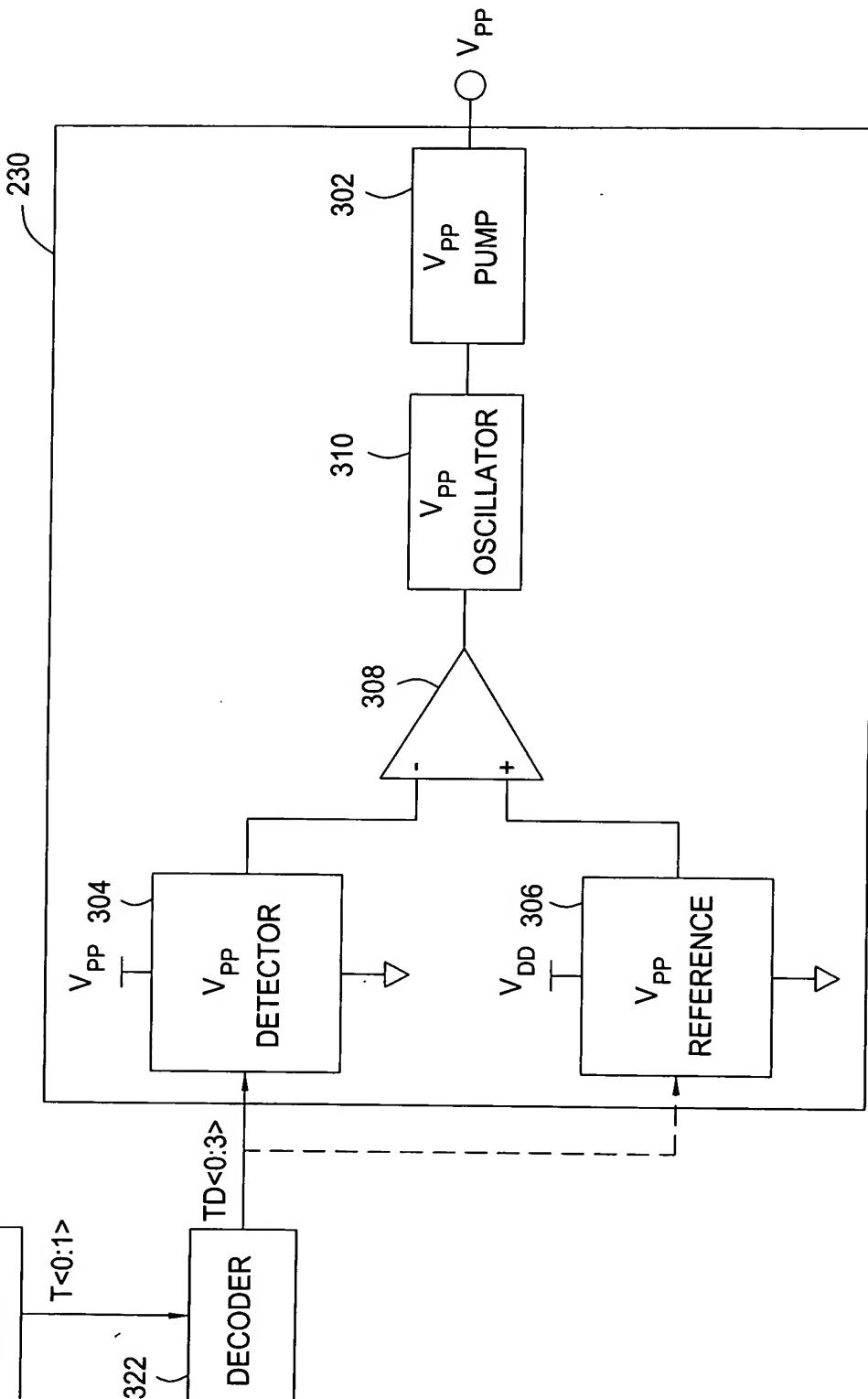


FIG. 2

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FIG. 3
320
322
TD<0:3>
MODE REGISTER
DECODER



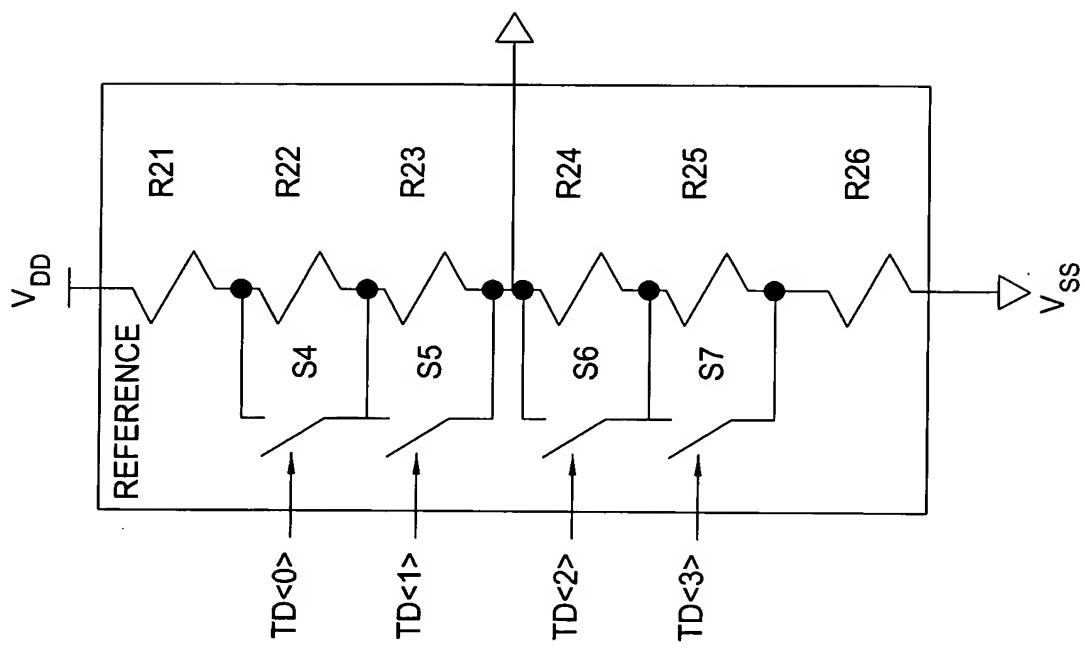


FIG. 4B

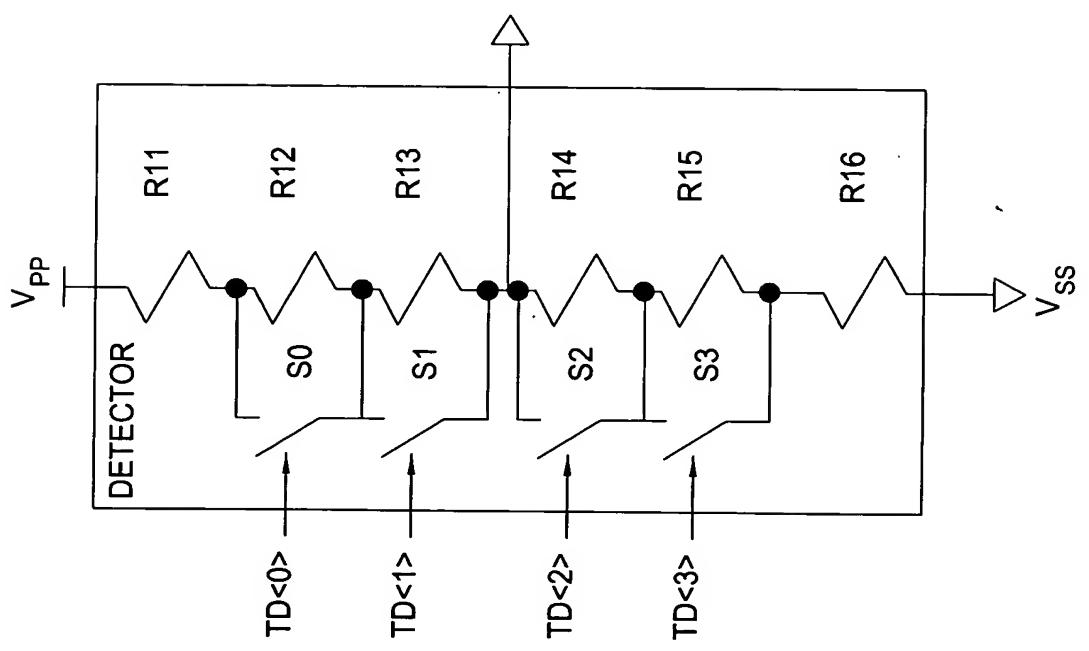


FIG. 4A

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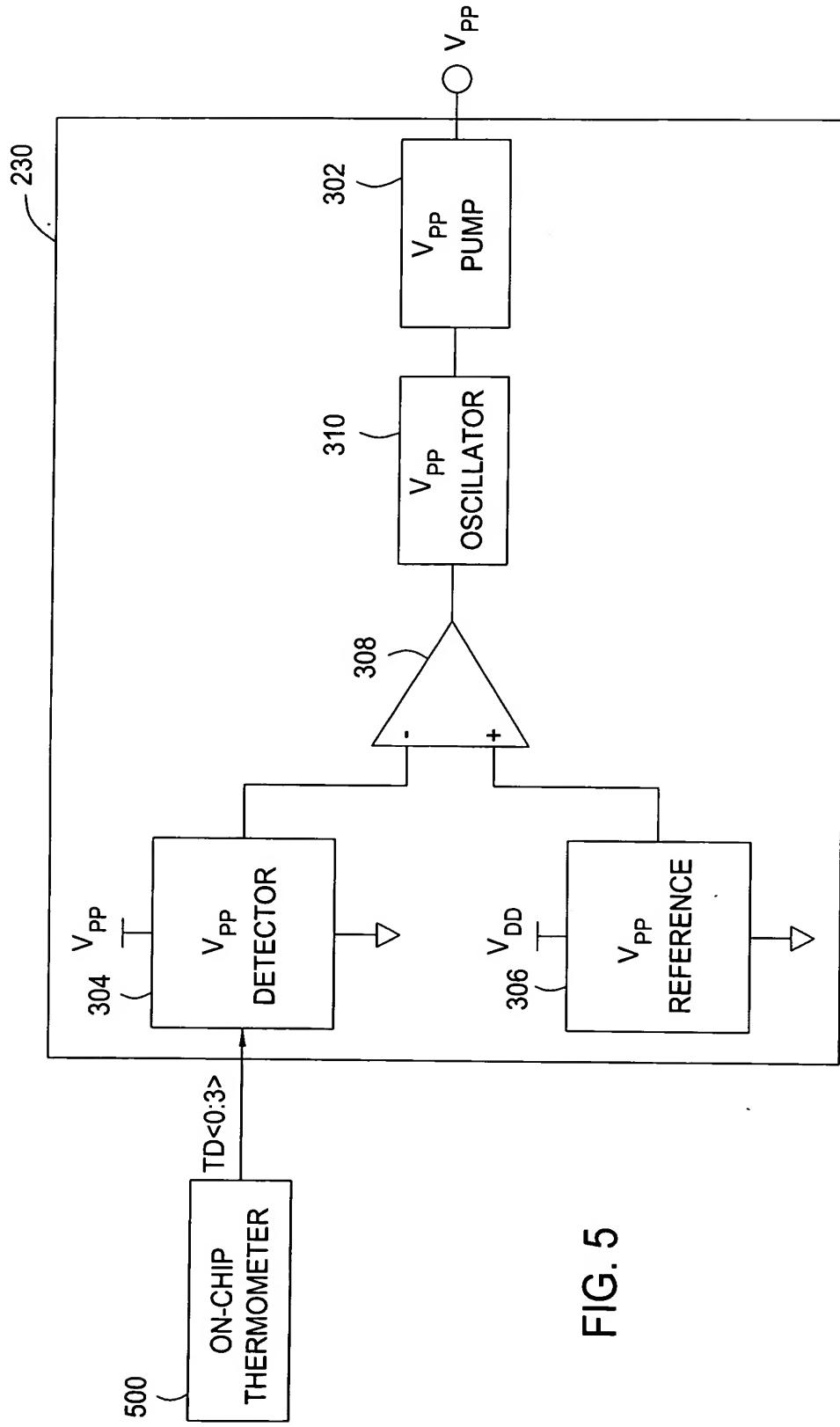


FIG. 5

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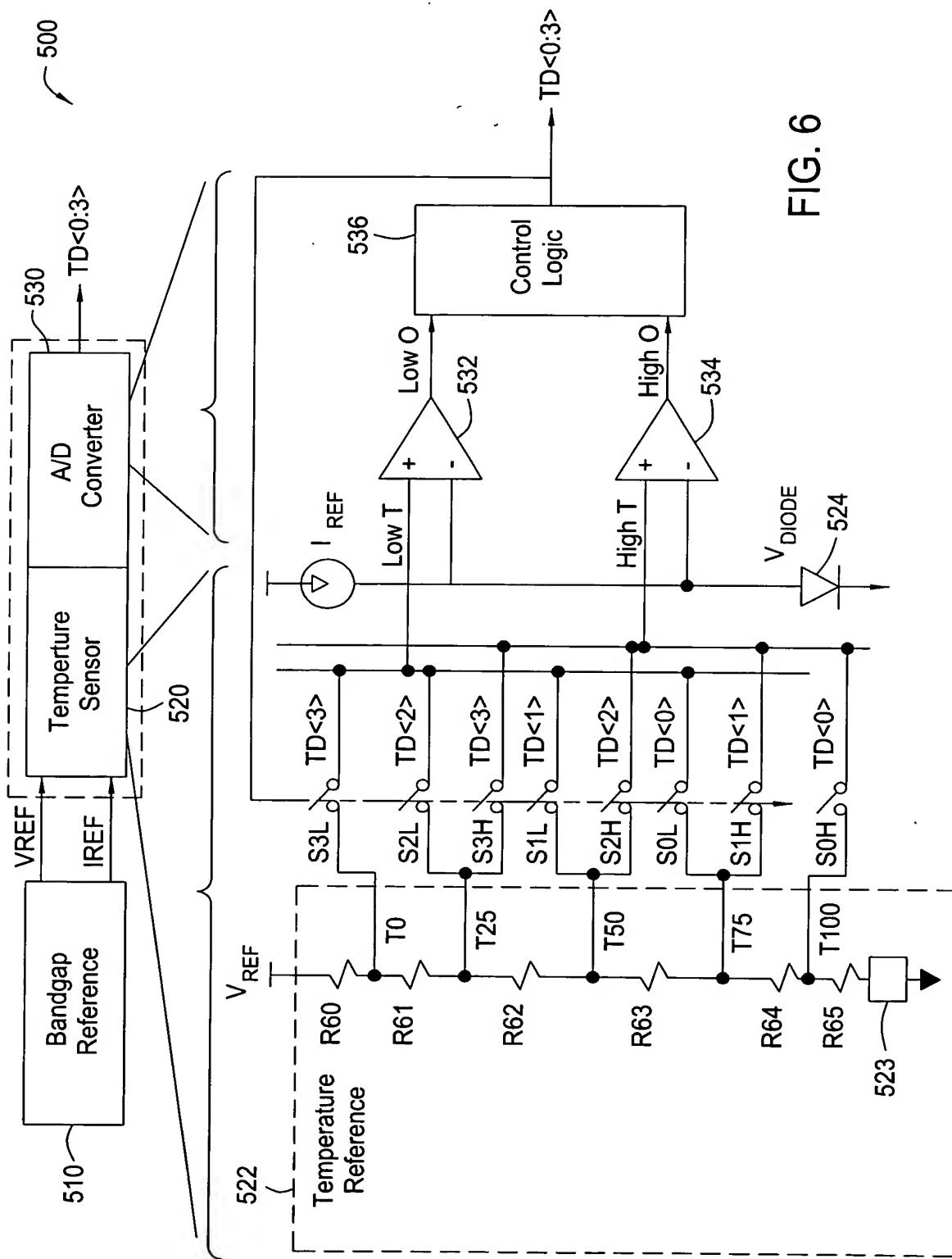


FIG. 6

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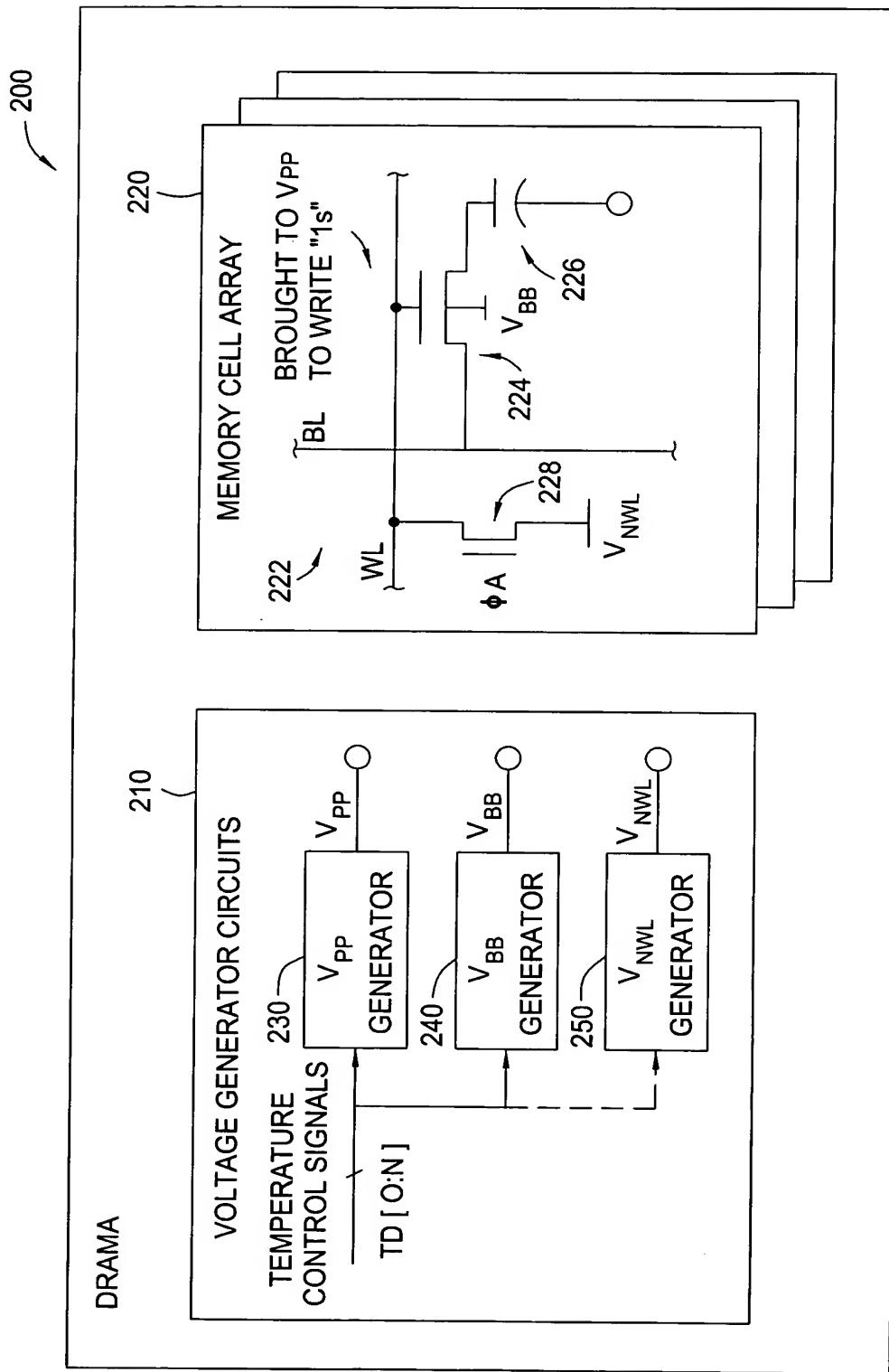


FIG. 7

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